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REMARKS

Applicant notes with appreciation that claims 1-4 and 6-8 were allowed and claims 10-14 and 18 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, claims 9, 15-17, 19 and 20 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Application No. US 2002/0180685 A1 ("Itakura et al.") in view of U.S. Patent Application No. 2002/0000969 A1 ("Ozawa"). In addition, claim 19 was objected to because of alleged informalities.

With respect to the objection of claim 19, Applicant has amended claim 19 to overcome the alleged informalities. With respect to the rejection of claims 9, 15-17, 19 and 20, Applicant respectfully asserts that the independent claims 9 and 16 are not obvious in view of the cited references of Itakura et al. and Ozawa, as explained in detail below. In view of the following remarks, Applicant respectfully requests that the independent claims 9 and 16, as well as the dependent claims 10-15 and 17-20, be allowed.

A. Patentability of Independent Claims 9 and 16

In the latest Office Action, the independent claims 9 and 16 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Itakura et al. in view of Ozawa. However, the Examiner has failed to establish a *prima facie* case of obviousness for claims 9 and 16. In particular, there is no valid suggestion or motivation to combine the teachings of Itakura et al. and Ozawa in the manner suggested by the Examiner. Thus, Applicant respectfully asserts that the independent claims 9 and 16 are not obvious in view of the cited references of Itakura et al. and Ozawa, and requests that these independent claims be allowed.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable

expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

On page 3 of the Office Action, the Examiner correctly states that "Itakura does not mention a memory connected to the control terminal of the output transistor, the memory being configured to store a signal on the control terminal from a previous operating cycle in which the output transistor was activated." However, the Examiner further states that "Ozawa teaches a memory being configured to store a signal from the previous operating cycle (*See page 12, claim 6: second line memory; See figure 9, 330: second line memory*)." The Examiner then states that "it would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a memory connected to the control terminal of the output transistor, the memory being configured to store a signal on the control terminal from a previous operating cycle in which the output transistor was activated, as taught by Ozawa, to the driving circuit of Itakura, so as to generate a determination signal with a simple structure."

Thus, the alleged suggestion or motivation to combine the teachings of Itakura et al. and Ozawa to derive the claimed invention appears to be "so as to generate a determination signal with simple structure." This statement may be a valid suggestion or motivation to use the control circuit 300' of Ozawa with the first line memory 320, the second line memory 330, the comparison circuit 340' and the determination memory 350', as shown in Fig. 9. However, such a statement is NOT a suggestion or motivation to modify the circuit of Itakura et al. by "inserting a second line memory at the node common to the gate of the output transistor (*Mp43*), feedback capacitor (*Cf1*), and switch (*Mn42*)," as suggested by the Examiner. There is no suggestion or motivation to use the second line memory 330 of Ozawa in any device other than the control device of Ozawa. Furthermore, the cited reference of Ozawa describes the second line memory 330 operating with the first line memory 320 and the comparison circuit 340'. There is no suggestion or motivation found in the cited references to use the second line memory 330 in an environment outside of the control device of Ozawa, especially in an amplifier or driving circuit, such as the circuit of Itakura. Specifically,

there is no suggestion or motivation found in the cited references to connect the second line memory 330 of Ozawa to an output transistor of a driving circuit, such as the output transistor Mp43 of the circuit of Itakura et al.

Furthermore, it is not logical to insert the second line memory 330 of Ozawa into the circuit of Itakura et al. "at the node common to the gate of the output transistor (*Mp43*), feedback capacitor (*Cf1*), and switch (*Mn42*)." If the second line memory 330 is inserted at this common node of the circuit of Itakura et al., where would all the input and output lines of the second line memory be connected to? Moreover, since the second line memory 330 requires control signals, where would the control signals come from? Furthermore, if the second line memory 330 is inserted at the common node of the circuit of Itakura et al., there is uncertainty as to whether the modified circuit would even work. Therefore, it is NOT obvious to one of ordinary skill in the art at the time the invention was made to modify the circuit of Itakura et al. by inserting the second line memory 330 of Ozawa into the circuit of Itakura et al., as suggested by the Examiner. As such, Applicant respectfully requests that the independent claim 9 be allowed.

The above remarks are also applicable to the independent claim 16, which includes the limitation of "*applying a stored signal to an output transistor in response to said input signal to produce an output signal on an output node.*" Since there is no valid suggestion or motivation to combine the teachings Itakura et al. and Ozawa in the manner suggested by the Examiner, the independent claim 16 is also not obvious in view of these cited references. As such, Applicant respectfully requests that the independent claim 16 be allowed as well.

B. Patentability of Dependent Claims 10-15 and 17-20

Each of the dependent claims 10-15 and 17-20 depends on one of the independent claims 9 and 16. As such, these dependent claims include all the limitations of their respective base claims. Therefore, Applicant submits that these dependent claims are allowable for at least the same reasons as their respective base claims.

Applicant respectfully requests reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,
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